Benefits of Stacked-Wafer Capacitors for High-Frequency Buck Converters

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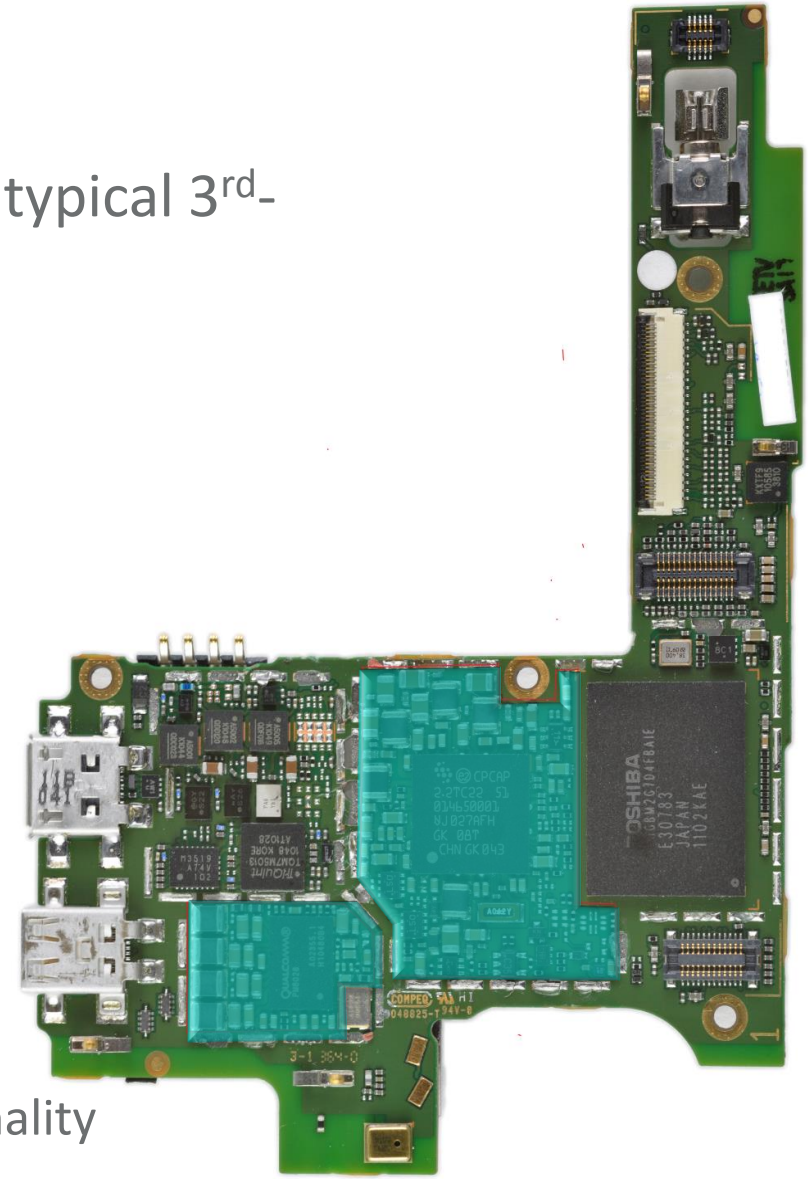
Mobile Device Trends

- Power Management occupies 30% of a typical 3rd-Generation Smartphone

- Many power supplies required today:
  - > Battery charger
  - > Fuel gauge
  - > Touch interface
  - > Backlight power

- More will be required in the future:
  - > Higher number of cores
  - > More discrete sensor modules and functionality
  - > Diverse radios and modes
  - > Wearable and medical technologies



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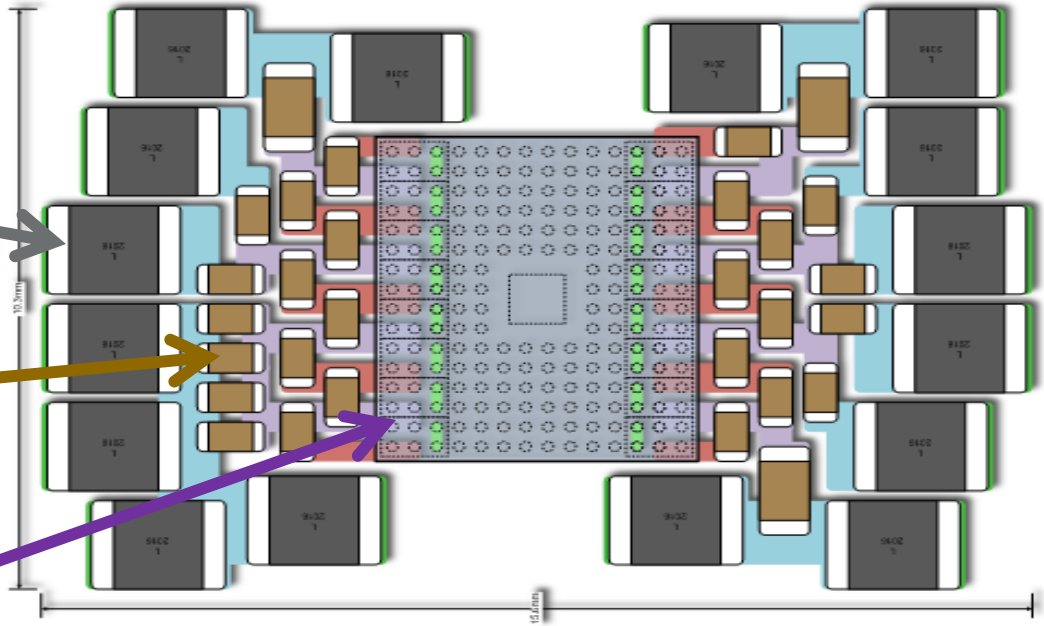
Mobile Power Conversion PCB Area:

Inductors
~60%

Capacitors
~20%

Chip Scale IC
~20%



5-10 High Efficiency Bucks

10-15 Low Noise LDOs

5-port Battery Charger

Low Noise PA Buck

Flash Memory Buck

5-10A CPU Buck

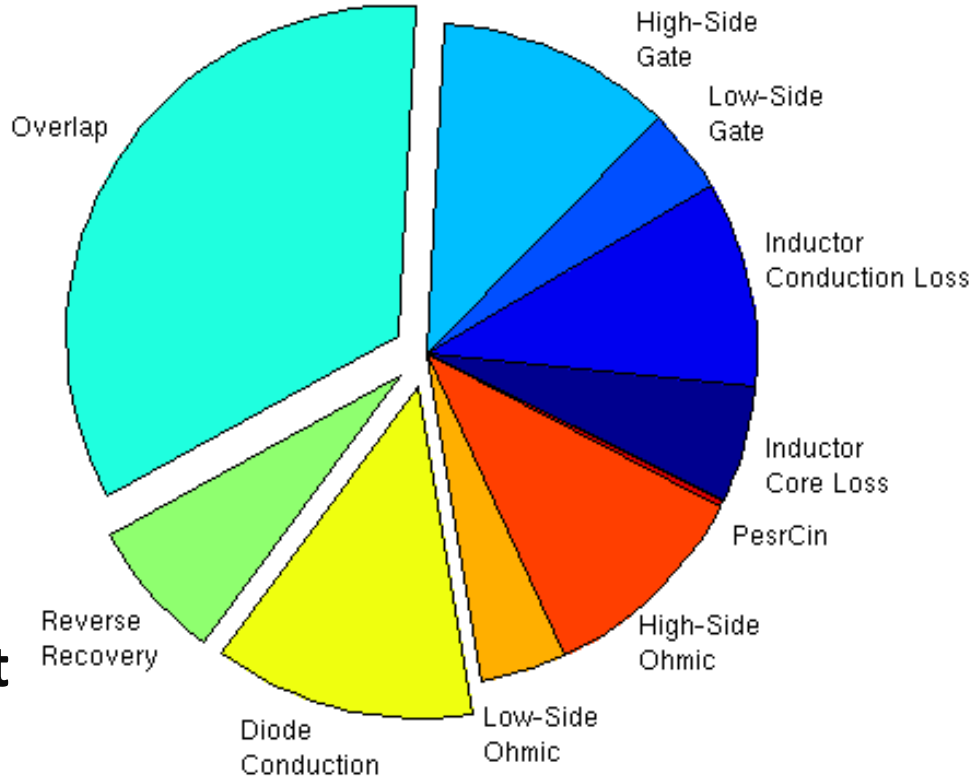
Backlight Power

- → Many rails are required to provide optimal power for each load.
- → Majority of the area is occupied by passive components which don't shrink with Silicon process node.
- → Typically we would shrink passive components by increasing switching frequency, but resulting efficiency penalty is unacceptable.

Optimized Buck Converter Losses

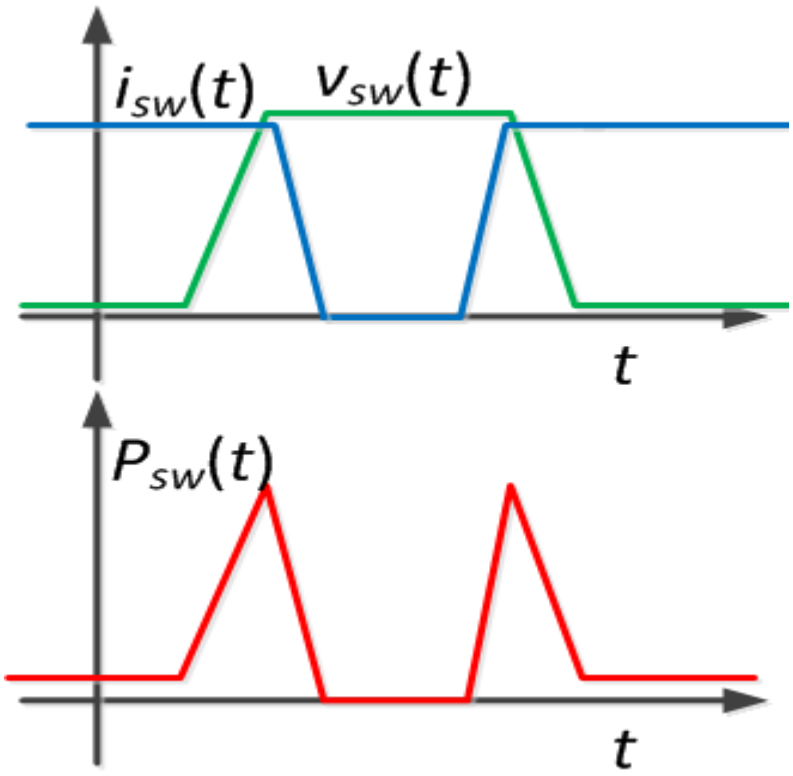
Power Loss Contributors Growing with Frequency:

- Turn-On and Turn-Off Commutation “Overlap”
- Reverse Recovery
- Body Diode Conduction
- Gate charge CV^2



→ Focus on reducing interconnect parasitics to enable higher frequency operation while minimizing efficiency penalties.

Turn-On and Turn-Off Commutation "Overlap"



Power FETs carry full current while withstanding full voltage

- **High dissipation**
- **High stress**
- **EMI source**

Turn-Off Transition Overlap:

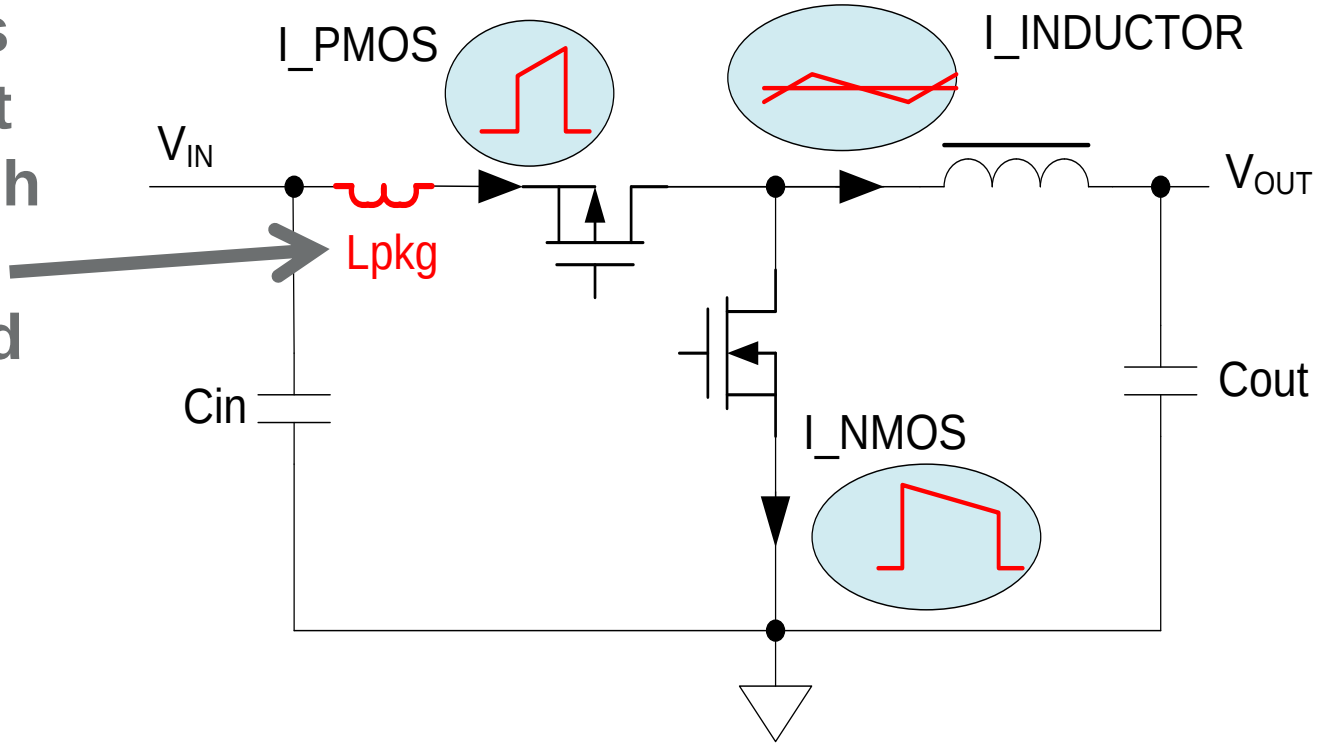
$$P_{overlapF} = f \cdot \frac{1}{2} \cdot V_{in} \cdot I_{peak} \cdot t_{2f} + f \cdot \frac{1}{2} \cdot V_{in} \cdot t_{1f} \cdot \max\left\{ I_{peak} - \frac{C_{LX} \cdot V_{in}}{t_{1f}}, 0 \right\}$$

Turn-On Transition Overlap:

$$P_{overlapR} = f \cdot \frac{1}{2} \cdot V_{in} \cdot I_{valley} \cdot t_r + f \cdot \frac{1}{2} \cdot C_{LX} \cdot V_{in}^2$$

Buck Converter – Input Loop Parasitic Inductance

Fast edge rates of input current passing through package inductance lead to ringing, EMI, and additional FET voltage stress.



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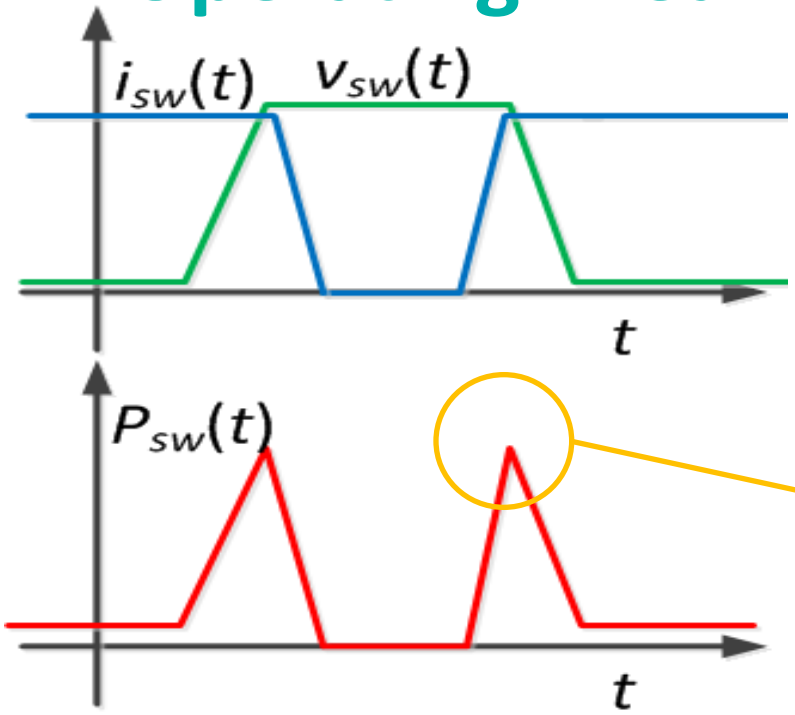
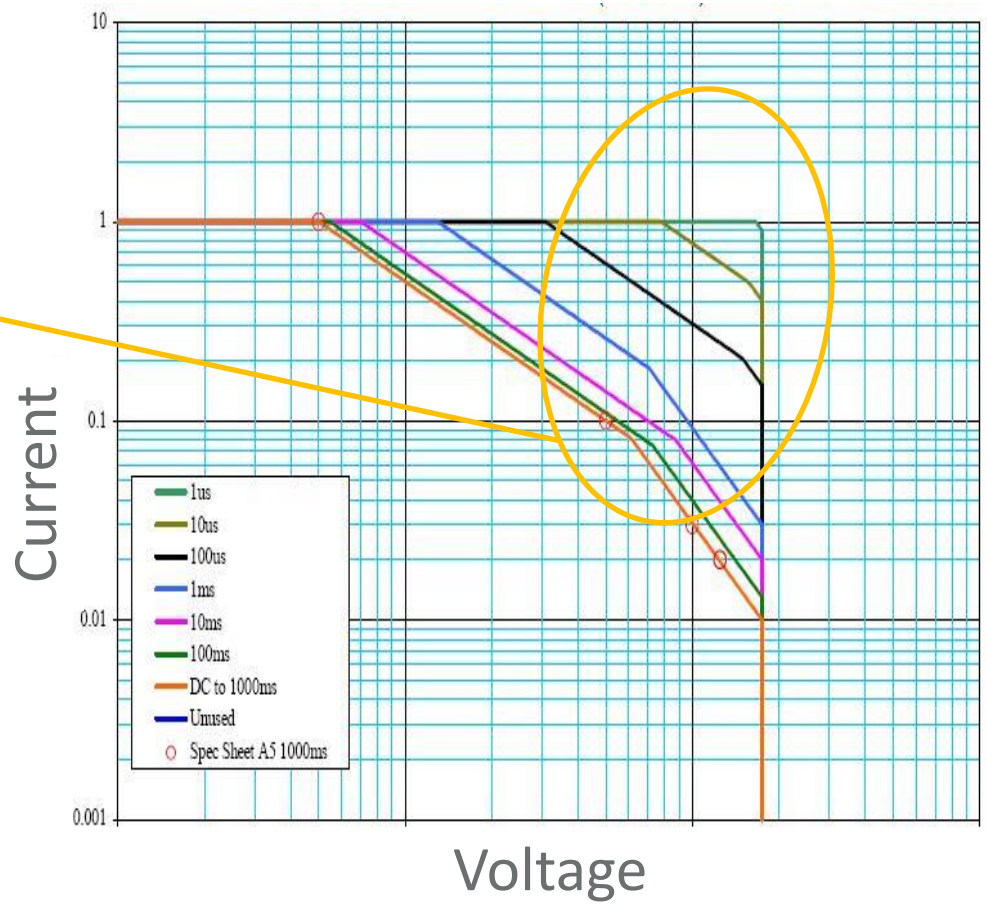
Turn-On and Turn-Off Commutation – Safe Operating Area



Voltage rating dictated by peak stresses, even though duration is very short

In practice, required design margin is 30-50%

Typical SOA Family of Curves for a Power MOSFET



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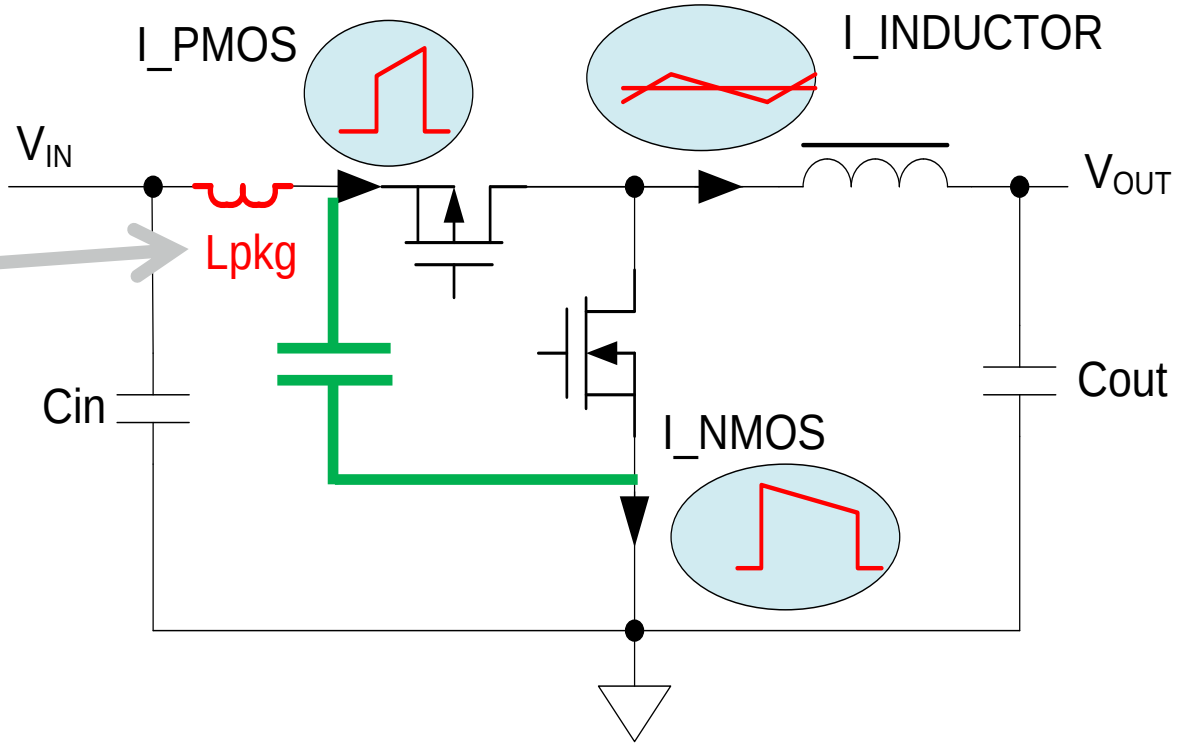
Turn-On and Turn-Off Commutation – Integrated Capacitor

Fast edge rates of input current passing through package inductance lead to ringing, EMI, and additional FET voltage stress.

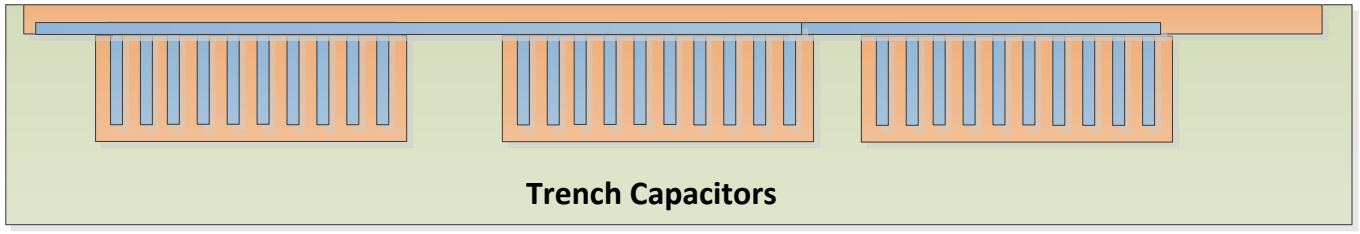


On-chip Cin can reduce parasitic inductance and SOA stress, allow faster commutation, increase efficiency.

On-Chip Input Capacitor - Candidates

Capacitor Type	Structure	Density at 5V (90nm)	Parasitic ESL
MOM CAP	Metal fringing capacitance	0.1-0.2 fF / μm^2	< 100pH
MOS CAP	MOSFET Gate Oxide	1-2 fF / μm^2	< 100pH
MIM CAP	Dedicated metal-insulator-metal sandwich	1-2 fF / μm^2	< 100pH
Full Stack	**MOS + MIM + 4 x MOM**	**2.5 - 5 fF / μm^2**	< 100pH
Discrete Chip Capacitor	eMGA package, low profile	0.5uF 0402 = 1µF / mm^2 1000fF / μm^2	~500pH
Discrete Chip Capacitor	On PCB, 1mm height	1uF 0402 = 2µF / mm^2 2000fF / μm^2	~1-2nH

Trench Capacitor Technology



Not to scale

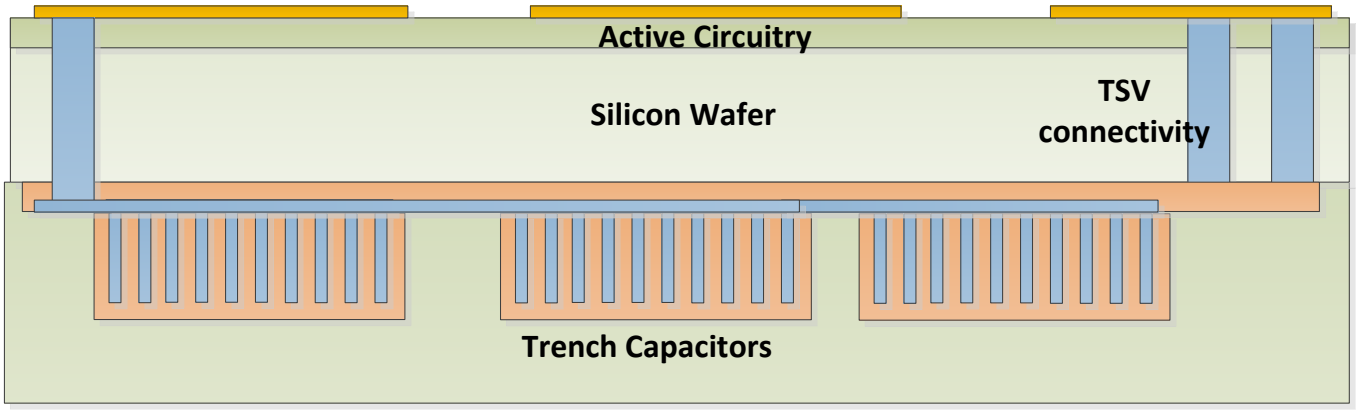
- Wafer-scale Silicon Trench Capacitor Technology:

  600 fF/µm^2 @ 5.5 MOV, TDDB 10 year; V_{BD} 19V,

  1000fF/µm^2 @ 3.3 MOV, TDDB 10 year; V_{BD} 11V,

Arkadii V. Samoilov, et. al, “3D Heterogeneous Integration for Analog”, IEEE. 2013.

Wafer-scale Integration



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- Wafer-wafer bonding + TSV connectivity between die
- Reduces interconnect inductance by up to 10x compared to traditional PCB.

On-Chip Input Capacitor - Candidates

Capacitor Type	Structure	Density at 5V (90nm)	Parasitic ESL
MOM CAP	Metal fringing capacitance	0.1-0.2 fF / um^2	< 100pH
MOS CAP	MOSFET Gate Oxide	1-2 fF / um^2	< 100pH
MIM CAP	Dedicated metal-insulator-metal sandwich	1-2 fF / um^2	< 100pH
Full Stack	MOS + MIM + 4 x MOM	2.5 - 5 fF / um^2	< 100pH
Trench capacitor with TSV integration	**Deep Reactive-Ion Etched**	**600fF / um^2**	**~100pH**
Discrete Chip Capacitor	eMGA package, low profile	0.5uF 0402 = 1uF/mm^2 1000 fF/um^2	~500pH
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Integrated Capacitor Benefits #1: Higher Input Voltage

Maximum operating voltage for various input bypass capacitor configurations

External C	Internal C	Max V_{IN}
1uF	0uF	6.6V
22uF	0uF	6.7V
0.5 uF	0.5 uF	7.6V
0uF	0.5uF	7.4V

Nominal Design – external C_{IN}.

Increasing C_{IN} does not help!

After moving half of the C_{IN} inside.

Less C_{IN} is required when integrated.

20% Increase in voltage headroom can enable device FOM improvement by 40%.

Integrated Capacitor Benefit #2: Higher Output Current

Maximum output current for various input bypass capacitor configurations

External C	Internal C	Max I_{OUT}	
1uF	0uF	350mA	Nominal Design – external C_{IN}.
0.5 uF	0.5 uF	550mA	After moving half of the C_{IN} inside.
0uF	1.0uF	900mA	More I_{out} is possible when C_{IN} is integrated.

Integrated Capacitor Benefit #3: Lower EMI

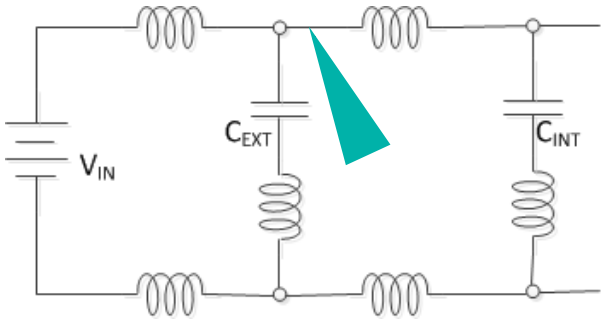
Conducted EMI performance for various input bypass capacitor configurations

External C	Internal C	EMI at 4*Fsw	EMI at 8*Fsw	Relative P_{TOTAL} (BW=500MHz)
1 uF	0 uF	4.8 mV	2.7 mV	1
0.5 uF	0.5 uF	1.6 mV	0.8 mV	0.12
0 uF	1.0 uF	2.9 mV	1.3 mV	0.43

Nominal Design – external C_{IN}.

Lowest EMI by partitioning C_{IN}.

Moving C_{IN} inside improves EMI.



- Partitioning C_{IN} creates a higher-order Pi-network effect – 4th order roll-off.

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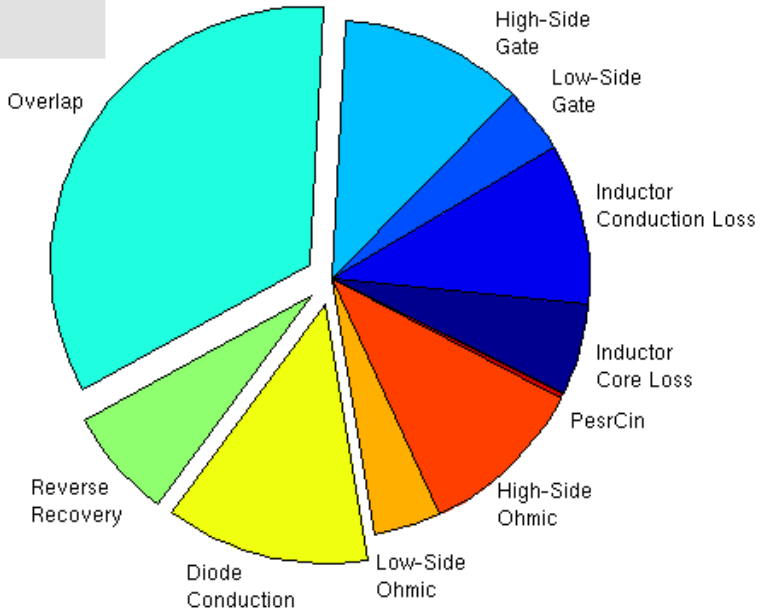
Integrated Capacitor Benefit #4: Minimal Frequency Impact (!)

Switching frequency increase enabled by integrated C_{IN}, for constant efficiency.

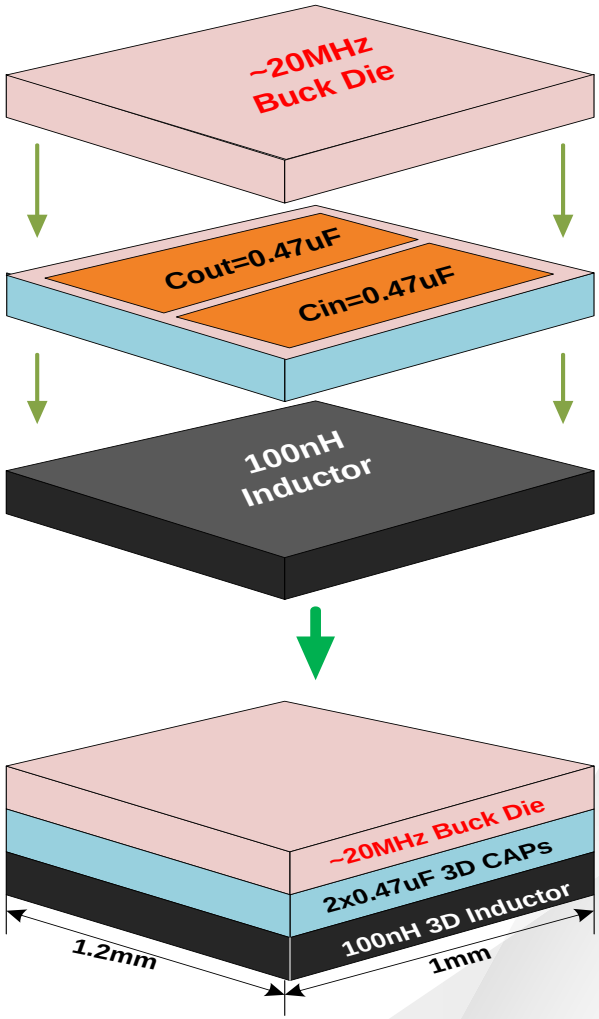
	4X Gate Drive (Measured)	4X Gate Drive (Theory)
$C_{internal}$ = 880nF $C_{external}$ = 0nF	+ 9%	+ 9.5%

- Input capacitor integration enable faster commutation resulting in higher efficiency.
- However, other loss mechanisms still increase with switching frequency.



Summary

- Integrated capacitors can improve DC-DC converter performance:
  - > 20% higher input voltage capability
  - > Increased output current capability (lower supply noise)
  - > Reduced conducted EMI
- Demonstrated a low-ESL, high-density capacitor technology.
- Next Steps:
  - > Address additional switching losses with new topologies and control.
  - > Integrated inductors…



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Thank You!